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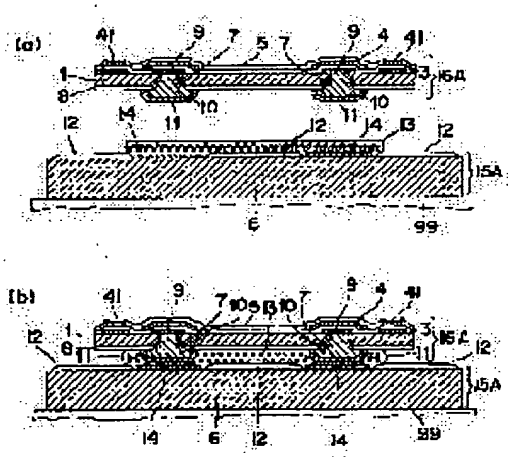
(54) SEMICONDUCTOR CHIP AND MULTI-CHIP SEMICONDUCTOR MODULE

(57)Abstract:

PURPOSE: To provide a multi-chip semiconductor module in which the mounting density per unit volume can be enhanced and which has excellent response characteristics, low cost, small restrictions in chip design and product design with repair of a defective chip.

CONSTITUTION: A semiconductor chip 16A is formed with a through hole 7 reaching the rear surface of an electrode pad 9 from the rear surface side of a substrate 1, and with a metal bump 10 protruding to the rear side via the hole 7 in contact with the rear surface of the pad 9. The chip 16A is provided in the state that stacked on another semiconductor chip 15A having an electrode pad 14 at the front side of a substrate 6. The metal bump 10 of the chip 16A is connected to the pad 14 of the chip 15A via an anisotropic conductive film 13 opposed to each other.



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* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Industrial Application] This invention relates to a multichip semi-conductor module with the structure where two or more semiconductor chips were accumulated. Moreover, it is related with the semiconductor chip used for constituting such a multichip semi-conductor module.
[0002] In addition, the multichip semi-conductor module of this invention differs from a device with which the semiconductor chip has been arranged to both sides of the leadframe of one sheet in that the laminating of the semiconductor chips is carried out. Moreover, the multichip semi-conductor module of this invention differs from the so-called three-dimension IC (integrated circuit) by which each semiconductor chip is constituted from a point formed as each chip by the wafer process on one semi-conductor substrate by carrying out the laminating of a wiring layer or the layer insulation layer one by one.
[0003]
[Description of the Prior Art] A multichip semi-conductor module is divided roughly into what arranged the semiconductor chip two-dimensional, the thing which accumulated the semiconductor chip and was arranged in three dimension, and the thing which takes the arrangement which compounded them. Moreover, it is classified according to by what kind of method the electrode of each semiconductor chip is connected.
[0004] As a multichip semi-conductor module of a two-dimensional array, the thing of the COB (chip on-board regulation) method which carried out direct continuation of the electrode of a semiconductor chip, for example to the printed circuit board by wirebonding is known. This COB method is used for comparatively cheap consumer products, such as memory card, for many years. Moreover, a semiconductor chip is once mounted with a TAB (tape automated bonding) method, and what connected the lead to the printed circuit board, the ceramic substrate, and the silicon substrate by soldering or alloy junction is put in practical use. Moreover, the metal bump who consists of solder metallurgy, nickel copper, etc. is formed on the electrode pad of a semiconductor chip, and what carried out face down bonding to the printed circuit board, the ceramic substrate, and the silicon substrate, and was connected to them (flip chip method) is known. This flip chip method is used until it results [from the device for computers] in consumer products, such as memory card, (JP,63-42157,A etc.). Of course, there is much what was mounted combining two or more of these connection techniques (JP,04-44256,A etc.).
[0005] As a multichip semi-conductor module of a three-dimension-array, the thing which ** U.S. N chip (nCHIP) company developed and which accumulated the semiconductor chip with small size through adhesives etc. on the semiconductor chip with large size, and connected the electrode pads of an up-and-down chip by wirebonding is famous. Moreover, **TCP (tape career package) is accumulated and there are some which connected the leads of each TCP (JP,01-309362,A, Taira 02-134859). Moreover, there are some which connected the electrodes of each chip with this metal in piles about a semi-conductor wafer with what embedded this through hole for the semi-conductor wafer which prepared the through hole on ** semi-conductor wafer with the metal in piles, and connected the electrodes of each chip (JP,63-213943,A), and the through hole embedded with the metal on ** semi-conductor wafer (JP,05-55454,A). moreover, ** -- what substituted the trench (slot) for some or all of these through holes is proposed (JP,05-41478,A, JP,05-198738,A).

[0006]
[Problem(s) to be Solved by the Invention] There are the following problems in the above-mentioned conventional multichip semi-conductor module.
[0007] first, the multichip semi-conductor module of a two-dimensional array -- the above -- even if it is the thing of which method, a limitation is in the packaging density per unit area. It is less than the thing of a three-dimension-array as for a thing of the flip chip method which a consistency goes up most. Moreover, since wiring which leads to the electrode of a chip is prolonged in the direction of a flat surface and becomes long, there is a problem that the response characteristic over a RF is not good.
[0008] Moreover, what accumulated the semiconductor chip among the multichip semi-conductor modules of a three-dimension-array, and connected the electrodes of an up-and-down chip by wirebonding (the above-mentioned **) cannot remove a wire easily, when a defect chip exists, but it has the problem that repair (activity of exchange etc.) of a defect chip cannot be performed. Moreover, since it is necessary to form an electrode pad around the location in which wirebonding is possible, i.e., a chip, the constraint on a chip design becomes large. Moreover, there is a problem that mounting time amount becomes comparatively long and mounting cost becomes high as a wire connection number increases.
[0009] Moreover, although repair of a defect chip is possible, since what accumulated TCP and connected the leads of each TCP (the above-mentioned **) once mounts each semiconductor chip in TCP, packaging density becomes low and it has the problem that mounting cost costs dearly. Moreover, it is difficult to pile up two or more TCP from which size differs, and the constraint on a product design is large.
[0010] Moreover, since what connected the electrodes of a chip for the semi-conductor wafer with the metal in a through hole or a trench in piles (the above-mentioned **, **, **) is embedding the through hole and the trench with the metal, it cannot perform repair of a defect chip. Moreover, since a laminated structure is formed in a wafer process, a wafer process is complicated and chip cost costs dearly. And there is no freedom in which the semiconductor chip of various classes can be combined in an assembly process, and a product design has constraint.
[0011] Then, the purpose of this invention is to offer the multichip semi-conductor module which can raise the packaging density per unit volume, can be excellent in a response characteristic, can repair a defect chip, and can reduce cost, and can lessen constraint on a chip design and a product design. Moreover, it is in offering the semiconductor chip suitable for constituting such a multichip semi-conductor module.
[0012]
[Means for Solving the Problem] In order to attain the above-mentioned purpose, it has the electrode pad prepared in the front-face side of a substrate and this substrate, the through hole which arrives at the rear face of the above-mentioned electrode pad from the rear-face side of this substrate at the above-mentioned substrate is formed, and a semiconductor chip according to claim 1 contacts the above-mentioned rear face of the above-mentioned electrode pad, and is characterized by to be prepared the metal bump who projects in the rear-face side of the above-mentioned substrate through the above-mentioned through hole.
[0013] Moreover, the semiconductor chip according to claim 2 is characterized by being covered by the deposit which the exposure by the side of the above-mentioned metal bump's above-mentioned substrate rear face becomes from the ingredient of the low melting point rather than the above-mentioned metal bump's ingredient in the semiconductor chip according to claim 1.
[0014] Moreover, a multichip semi-conductor module according to claim 3 It has the semiconductor chip of 1 according to claim 1 or 2 in the condition of having been put on another semiconductor chip which has an electrode pad in the front-face side of a substrate. With the above-mentioned metal bump by the side of the rear face of the semiconductor chip of the above 1 It is characterized by for the above-mentioned electrode pad by the side of the front face of the semiconductor chip which consists in top Norikazu's semiconductor chip bottom countering mutually, and connecting it through the anisotropy electric conduction film.
[0015] Moreover, the multichip semi-conductor module according to claim 4 is characterized by having an electrode pad in the condition of having been put on another semiconductor chip which it has, and connecting the above-mentioned metal bump and the above-mentioned electrode pad to the front-face side of a substrate through the above-mentioned deposit in the semiconductor chip of 1 according to claim 2.
[0016] Moreover, the multichip semi-conductor module according to claim 5 is characterized by preparing the

deposit which consists of an ingredient of the above-mentioned metal bump's deposit, and an ingredient which can form an alloy in the front face of the above-mentioned electrode pad of the semiconductor chip which consists in the above bottom in the multichip semi-conductor module according to claim 4.
[0017]
[Function] The semiconductor chip of claim 1 has the metal bump who projects in the rear-face side of a substrate while having an electrode pad in the front-face side of a substrate. A multichip semi-conductor module like claim 3 is constituted simply and easily in this semiconductor chip by following by accumulating an electrode pad on the front-face side of a substrate on both sides of the anisotropy electric conduction film on another semiconductor chip which it has. Moreover, what accumulated two or more these semiconductor chips may be accumulated on another semiconductor chip which has an electrode pad in the front-face side of a substrate further, or a wiring substrate. In addition, a free combination is possible. Thus, according to this semiconductor chip, the multichip semi-conductor module of various classes is constituted simply and easily.
[0018] The semiconductor chip of claim 2 is covered by the deposit which the exposure by the side of the above-mentioned metal bump's above-mentioned substrate rear face becomes from the ingredient of the low melting point rather than the above-mentioned metal bump's ingredient. A multichip semi-conductor module like claim 4 is constituted simply and easily by following, for example, accumulating this semiconductor chip on another semiconductor chip which has an electrode pad in the front-face side of a substrate, and heating to the temperature which the above-mentioned deposit fuses. Moreover, what accumulated two or more these semiconductor chips may be accumulated on another semiconductor chip which has an electrode pad in the front-face side of a substrate further, or a wiring substrate. In addition, a free combination is possible. Thus, according to this semiconductor chip, the multichip semi-conductor module of various classes is constituted simply and easily.
[0019] Since it has the multichip semi-conductor module of claim 3 where the semiconductor chip of 1 of claim 1 or claim 2 and another semiconductor chip are able to be accumulated, the packaging density per unit volume increases as compared with the case where it once mounts in TCP when arranging a semiconductor chip two-dimensional. Moreover, since a metal bump becomes wiring which connects the electrodes of a chip, as compared with the case where wiring is prepared in the direction of a flat surface, the die length of wiring becomes short, and the response characteristic over a RF becomes good. Moreover, the connection with the electrode pad of the semiconductor chip which consists in 1 the metal bump and the bottom of a semiconductor chip may be canceled by dissolving the anisotropy electric conduction film used for connection. Therefore, repair of a defect chip is performed easily. Moreover, since a laminated structure is formed not in a wafer process but in an assembly process, chip cost is reduced. And since package bonding of the electrodes of a chip is done by the metal bump, mounting time amount becomes short. Moreover, without once mounting a semiconductor chip in TCP, each semiconductor chip is accumulated directly and this multichip semi-conductor module is constituted. Therefore, mounting cost is reduced with chip cost. Moreover, since wirebonding is not performed, an electrode pad may be prepared in the field of the arbitration in a chip, and there is little constraint on a chip design. And since the semiconductor chip of various classes can be combined in an assembly process, the constraint on a product design also decreases.
[0020] Since it has the multichip semi-conductor module of claim 4 where the semiconductor chip of 1 of claim 2 and another semiconductor chip are able to be accumulated, the packaging density per unit volume increases as compared with the case where it once mounts in TCP when arranging a semiconductor chip two-dimensional. Moreover, since a metal bump becomes wiring which connects the electrodes of a chip, as compared with the case where wiring is prepared in the direction of a flat surface, the die length of wiring becomes short, and the response characteristic over a RF becomes good. Moreover, connection with the electrode pad of the semiconductor chip which consists in above 1 the metal bump and the bottom of a semiconductor chip may be canceled by heating the semiconductor chip which consists in the above bottom from a rear-face side, and carrying out melting of the deposit which has covered the above-mentioned metal bump. Therefore, repair of a defect chip is performed easily. Moreover, since a laminated structure is formed not in a wafer process but in an assembly process, chip cost is reduced. And since package bonding of the electrodes of a chip is done by the metal bump, mounting time amount becomes short. Moreover, without once mounting a semiconductor chip in TCP, each semiconductor chip is accumulated directly and this

multichip semi-conductor module is constituted. Therefore, mounting cost is reduced with chip cost. Moreover, since wirebonding is not performed, an electrode pad may be prepared in the field of the arbitration in a chip, and there is little constraint on a chip design. And since the semiconductor chip of various classes can be combined in an assembly process, the constraint on a product design also decreases.
[0021] The deposit which consists of an ingredient of the above-mentioned metal bump's deposit and an ingredient which can form an alloy is prepared in the front face of the above-mentioned electrode pad of the semiconductor chip with which the multichip semi-conductor module of claim 5 consists in the above bottom. Therefore, the deposit of the metal bump of the semiconductor chip of the above 1 and the deposit of the electrode pad of the semiconductor chip which consists in the above bottom are contacted at the time of assembly, and connection is easily made by performing heating, pressurization, or its both.
[0022]
[Example] Hereafter, an example explains this invention to a detail.
[0023] First, the semiconductor chip of one example of this invention is explained.
[0024] Drawing 1 shows the production process of the semiconductor chip of one example.
[0025] ** First, as shown in this drawing (a), while forming active elements, such as an MOS transistor which is not illustrated, form in the with a thickness of 625 micrometers front-face side of a silicon substrate 1 the 1st metal wiring layer 2 which consists of aluminum, an interlayer insulation film 3, the 2nd metal wiring layer 4, and a protective coat 5 according to a CMOS (complementary MOS) process. In addition, 9 shows the electrode pad part of the 1st metal wiring layer 2, and 41 shows the electrode pad part of the 2nd metal wiring layer 4.
[0026] ** next, it is shown in this drawing (b) -- as -- a silicon substrate 1 -- predetermined thickness -- grind until it becomes the thickness of 40 micrometers preferably. As the polish approach, usual rear-face polish equipment (not shown) performs mechanical polishing first, it grinds until the thickness of a substrate 1 is set to 200 micrometers, and after that, it is in the condition from which the front-face side of a substrate 1 was protected in the wax 90 grade, and the rear-face side of a substrate 1 is performed by the approach of carrying out chemical etching using KOH, NaOH, or a FUTSU nitric acid further. Under the present circumstances, if the scribe line of a chip is also etched, it is not necessary to carry out dicing at the time of mounting.
[0027] ** Next, the coat of the photoresist 91 is carried out to the rear face of a substrate 1, perform exposure and development, remove the part corresponding to the electrode pad 9 among photoresists 91, and form opening 91a. As shown in this drawing (c) after an appropriate time, a substrate 1 is alternatively etched using KOH, NaOH, or a FUTSU nitric acid, and the through holes 7 and 7 which arrive at the rear face of the electrode pads 9 and 9 from the rear-face side of this substrate at a substrate 1 are formed. At this time, through holes 7 and 7 are finished from a rear-face side in the shape of [to which a cross-section dimension becomes small gradually toward a front-face side] a taper. There is a possibility that the area of the lobe of the metal bump which will be behind formed if it will become smaller [the area of opening 91a] than the area of the electrode pad 9 if it forms so that opening 91a may be located in the electrode pad 9 here, and a perpendicular through hole is formed to a substrate may also become small, a touch area with electrodes, such as other chips and a wiring substrate, may also become small, and suitable contact resistance may not be obtained. In this invention, opening of a through hole is made larger in area than the outcrop of the electrode pad 9, and the area of the contact section can be rationalized. Moreover, although it must carry out to more than comparable with the touch area which wishes the area of the electrode pad 9 and is not suitable for detailed-ization in order to secure the touch area of other electrodes and a metal bump if a through hole is made into a perpendicular configuration, area of the electrode pad 9 can be made small by considering as a taper configuration like this invention. Furthermore, to the pressurization at the time of connecting with electrodes, such as other chips, also when a load concentrates on a specific metal bump by dispersion in the height of the dispersion metallurgy group bump of the thickness of a substrate, it thinks, but even when a load higher than usual is added, since it has a taper in a through hole, a load will be responded to also not only in respect of the electrode 9 but in respect of a taper, and the damage to an electrode 9 can be eased.
[0028] ** next, CVD (chemical vapor deposition) as shown in this drawing (d), after exfoliating and removing a resist 91 -- form in the whole surface (the wall of a through hole 7 is included) the insulator layer 8 which becomes the rear face of a substrate 1 from SiO2, SiN, etc. by law etc. This insulator layer 8 turns into a

protective coat on the rear face of a chip. Then, as shown in this drawing (e), by dry etching, the part corresponding to the electrode pad 9 is removed among insulator layers 8, and the rear face of the electrode pad 9 is exposed.

[0029] In addition, as an approach of forming a protective coat in the rear face of a substrate 1, the coat of the resin, such as photosensitive polyimide, is carried out to the rear face of a substrate 1, exposure and development are performed, and there is also a method of removing only the part corresponding to the electrode pad 9.

[0030] ** Next, the substrate 1 of this condition is immersed in the electroless deposition liquid of Zn, and form Zn plating (not shown) with a thickness of 0.3-0.5 micrometers in the rear face of the electrode pad 9. This processing can remove the oxide film of aluminum side, and pure aluminum side can be secured to Zn plating interface. Then, as shown in this drawing (f), the substrate 1 of this condition is immersed in the temperature of 90 degrees C, and nickel electroless deposition liquid of ph4.5 for 2 hours, and the non-electrolyzed nickel plating 10 is grown up into the rear face of the electrode pad 9. Thereby, the rear face of the electrode pad 9 can be contacted and the nickel bump 10 who projected only 10 micrometers to the rear-face side of a substrate 1 through the through hole 7 can be formed. Furthermore, the Au deposits 11 and 11 with a thickness of 0.2 micrometers are formed in the nickel bumps' 10 and 10 exposure by non-electrolyzed Au plating. Although nickel bump is used as a metal bump, for others, it can be used as wiring and can be used, the metal, for example, the gold etc., etc. which does not cause deformation at the time of connection with other electrodes.

[0031] ** Finally, remove the wax 90 for protection by the side of the front face of a substrate 1, and complete a semiconductor chip 16. The electric test of this semiconductor chip 1 can contact a prober by the bumps 10 and 10 (correctly deposits 11 and 11) by the side of a chip rear face, and the usual circuit tester can perform it.

[0032] According to this semiconductor chip 16, the multichip semi-conductor module of various classes can be constituted simply and easily.

[0033] Next, the multichip semi-conductor module of one example of this invention is explained.

[0034] As shown in drawing 2 (b), where semiconductor chip 16A and semiconductor chip 15A of another class are able to be accumulated, it has this multichip semi-conductor module 20A.

[0035] Semiconductor chip 16A is the same as the semiconductor chip 16 of drawing 1 (g). On the other hand, semiconductor chip 15A forms the electrode pads 14 and 14 which consist of aluminum while forming in the front-face side of a silicon substrate 6 active elements, such as an MOS transistor which is not illustrated. The electrode pads 14 and 14 are formed in the location which corresponds with the nickel bumps 10 and 10 of semiconductor chip 16A. The part around the electrode pad 14 is covered by the protective coat 12 among the front faces of a substrate 6.

[0036] When assembling this multichip semi-conductor module 20A, as shown in drawing 2 (a), temporary attachment of the anisotropy electric conduction film 13 which uses thermosetting resin as a base material at the front-face side of semiconductor chip 15A is first carried out so that the electrode pads 14 and 14 may be covered. Next, semiconductor chip 15A is laid on a stage 99, and semiconductor chip 16A is moved to the upper part. And the horizontal position of semiconductor chip 16A is tuned finely, and it positions in the location where the nickel bumps 10 and 10 who projected to the rear-face side of semiconductor chip 16A, and the electrode pads 14 and 14 of semiconductor chip 15A counter mutually. Then, semiconductor chip 16A is moved below, it pushes against semiconductor chip 15A, and this sticking by pressure is performed. Sticking-by-pressure conditions are made into pressure [of 20kg/cm2], temperature [of 200 degrees C], and time amount 20 seconds. Thereby, as shown in drawing 2 (b), the nickel bumps 10 and 10 of semiconductor chip 16A and the electrode pads 14 and 14 of semiconductor chip 15A are connected through the anisotropy electric conduction film 13. Thus, an assembly is performed easily.

[0037] A prober is contacted to the external electrode pads 41 and 41 of semiconductor chip 15A after assembly completion, and an electric test is performed. When it becomes clear that one of semiconductor chips is faulty as a result of a test, the solvent for repair is poured in among semiconductor chips 16A and 15A, it exfoliates and the anisotropy electric conduction film 13 is removed. Thereby, connection between the nickel bumps 10 and 10 of semiconductor chip 16A and the electrode pads 14 and 14 of semiconductor chip 15A is canceled. Therefore, a defect chip can be repaired easily.

[0038] Moreover, since it has this multichip semi-conductor module 20A where semiconductor chips 16A and 15A are able to be accumulated, it can raise the packaging density per unit volume as compared with the case where it once mounts in TCP when arranging a semiconductor chip two-dimensional. That is, since semiconductor chip 16A has thickness of about 40 micrometers by polish, the thickness after piling up semiconductor chips 16A and 15A also becomes in the thing twist of the structure which piled up TCP, and it can make it thin. Therefore, a product can be miniaturized, when this multichip semi-conductor module is mounted and it uses for a product.
[0039] Moreover, since the metal bump 10 becomes wiring which connects electrode 14 comrades of a chip, the die length of wiring can be shortened as compared with the case where wiring is prepared in the direction of a flat surface, and the response characteristic over a RF can be improved.
[0040] Moreover, since each substrate ingredient of semiconductor chips 15A and 16A is silicon, even if an ambient temperature changes somewhat, it is hard to produce distortion between chip 15A by thermal expansion, especially the linear expansion of the direction of a substrate side, and 16A. Therefore, the dependability of connection can be raised as compared with the case where the chip which consists of a different substrate ingredient is connected.
[0041] Moreover, since a laminated structure is formed not in a wafer process but in an assembly process, chip cost can be reduced. And in an assembly process, since package bonding of the electrode 14 comrades of a chip is done by the metal bump 10, mounting time amount can be shortened. Moreover, without once mounting a semiconductor chip in TCP, each semiconductor chips 16A and 15A are accumulated directly, and this multichip semi-conductor module 20A is constituted. Therefore, mounting cost can be reduced with chip cost.
[0042] Moreover, since wirebonding is not performed in an assembly process, the electrode pad 14 may be formed in the field of the arbitration in a chip, and there is little constraint on a chip design. And since various semiconductor chips can be combined in an assembly process, constraint on a product design can also be lessened.
[0043] Next, modification 20B of the above-mentioned multichip semi-conductor module is explained.
[0044] As shown in drawing 3 (b), where semiconductor chip 16B and semiconductor chip 15B of another class are able to be accumulated, it has this multichip semi-conductor module 20B.
[0045] Semiconductor chip 16B is the semiconductor chip 16 of drawing 1 (g), and the thing of an abbreviation EQC. However, it replaces with the Au deposits 11 and 11 at the nickel bumps' 10 and 10 exposure, and differs in that the solder deposits 11B and 11B with a thickness of 5 micrometers are formed of non-electrolyzed solder plating.
[0046] On the other hand, semiconductor chip 15B is the thing of semiconductor chip 15A and an abbreviation EQC shown in drawing 2 (b). It differs in that the barrier metal layer 19 which consists of Ti/W, respectively, and the Au deposit 18 with a thickness of 0.5 micrometers are formed in the front face of the electrode pads 14 and 14 which consist of aluminum. In addition, 17 shows the whole electrode pad which has the Ti/W layer 19 and the Au layer 18 on the aluminum layer 14.
[0047] When assembling this multichip semi-conductor module 20B, as shown in drawing 3 (a), semiconductor chip 15B is laid on the stage 99 held at the temperature of 280 degrees C, and semiconductor chip 16B is moved to that upper part. And the horizontal position of semiconductor chip 16B is tuned finely, and it positions in the location where the nickel bumps 10 and 10 of semiconductor chip 16B and the electrode pads 17 and 17 of semiconductor chip 15B counter mutually. Then, semiconductor chip 16B is moved below and it lays on semiconductor chip 15B. Then, as shown in drawing 3 (b), nickel bump does not deform, but wrap solder deposit 11B fuses the nickel bumps 10 and 10, and the nickel bumps 10 and 10 of semiconductor chip 16B and the electrode pads 17 and 17 of semiconductor chip 15B are connected through solder 11B. Thus, an assembly is performed easily.
[0048] A prober is contacted to the external electrode pads 41 and 41 of semiconductor chip 15B after assembly completion, and an electric test is performed. When it becomes clear that one of semiconductor chips is faulty as a result of a test, it is in the condition to which the stage 99 was heated at 300 degrees C, and melting of the solder 11B was carried out, and semiconductor chip 16B and semiconductor chip 15B are made to estrange. Thereby, a defect chip can be repaired easily.

[0049] Moreover, like multichip semi-conductor module 20A shown in drawing 2 , this multichip semi-conductor module 20B can raise the packaging density per unit volume, can be excellent in a response characteristic, and can reduce cost, and can lessen constraint on a chip design and a product design.
[0050] Drawing 4 shows the multichip semi-conductor module 20 constituted by forming three laminated structures 20A, 20B, and 20C on the semiconductor chip 15 of large ** of one sheet.
[0051] Here, in addition to the electrode pad 14 used for constituting laminated structures 20A, 20B, and 20C, the electrode pads 21 and 21 are formed in the front face of the silicon substrate 6 which constitutes a semiconductor chip 15 at the outermost periphery.
[0052] The laminated structures 20A and 20B prepared in both sides among three laminated structures are the same structure as what was shown in drawing 2 and drawing 3 .
[0053] Laminated-structure 20C prepared in the center is equipped with two semiconductor chips 16E and 16D accumulated on the silicon substrate 6. In this field, the electrode pads 17 and 17 which are from the aluminum layer 14, the Ti/W layer 19, and the Au layer 20 on the front-face side of a silicon substrate 6 are formed. The electrode pads 17 and 17 are formed in the location which corresponds with the nickel bumps 10 and 10 of semiconductor chip 16E. Semiconductor chip 16E is the thing of semiconductor chip 16B and an abbreviation EQC shown in drawing 3 . However, it differs in that opening is prepared in the protective coat 5 on the 2nd metal wiring layer 4. Semiconductor chip 16D is the same as the semiconductor chip 16 of drawing 1 (g).
[0054] When assembling this laminated-structure 20C, first, semiconductor chip 16E lays semiconductor chip 16E on a stage 99, moves semiconductor chip 16D to that upper part, and is positioned in the location where the nickel bumps 10 and 10 of semiconductor chip 16D and the electrode pads 14 and 14 of semiconductor chip 16E counter mutually. Then, semiconductor chip 16D is moved below, it pushes against semiconductor chip 16E, and thermocompression bonding is performed. Next, the semiconductor chips 16E and 16D by which the laminating was carried out are positioned in the location where the nickel bumps 10 and 10 of semiconductor chip 16E and the electrode pads 17 and 17 by the side of a substrate 6 counter mutually, and are laid on the substrate 6 heated by the temperature of 280 degrees C. Then, wrap solder deposit 11B fuses the nickel bumps 10 and 10 of semiconductor chip 16E, and the nickel bumps 10 and 10 of semiconductor chip 16E and the electrode pads 17 and 17 of a substrate 6 are connected through solder 11B. Thus, this laminated-structure 20C is assembled easily.
[0055] As the laminated structures 20A and 20B prepared in both sides were also already described, it is assembled easily. Therefore, this multichip semi-conductor module 20 whole is assembled easily.
[0056] After assembly completion, about each laminated structures 20A, 20B, and 20C, a prober is contacted to the external electrode pads 41 and 41 of the semiconductor chips 16A, 16B, and 16D which consist in the bottom, respectively, and an electric test is performed. When it becomes clear that the defect chip is included in laminated-structure 20A as a result of a test, the solvent for repair is poured in between semiconductor chip 16A and a substrate 6, it exfoliates and the anisotropy electric conduction film 13 is removed. Thereby, connection between the nickel bumps 10 and 10 of semiconductor chip 16A and the electrode pads 14 and 14 of a substrate 6 is canceled. Moreover, when it becomes clear that the defect chip is included in laminated-structure 20B, it is in the condition to which the substrate 6 was heated at 300 degrees C, and melting of the solder 11B was carried out, and semiconductor chip 16B and a substrate 6 are made to estrange. Moreover, when it becomes clear that the defect chip is included in laminated-structure 20C, it is in the condition to which the substrate 6 was similarly heated at 300 degrees C, and melting of the solder 11B was carried out, and semiconductor chips 16D and 16E are made to estrange from a substrate 6 with a laminating condition. Thereby, a defect chip can be repaired easily.
[0057] Moreover, like a laminated-structure 20A and 20B independent case (drawing 2 , drawing 3), this multichip semi-conductor module 20 can raise the packaging density per unit volume, can be excellent in a response characteristic, and can reduce cost, and the constraint on a chip design and a product design can lessen it.
[0058] Drawing 5 shows the condition of having mounted the multichip semi-conductor module 20 shown in drawing 4 by transfermold. A module 20 is in the condition which turned the semiconductor chip 15 down, and is attached in header unit 24a of a leadframe 24 by the connection material 25. The outermost periphery

electrode pad 21 of a semiconductor chip 15 and pin section 24b of a leadframe 24 are connected by the wire 22 with the wirebonding method. And except for the tip of pin section 24a, the mold of a module 20 and the leadframe 24 is carried out with resin 23.

[0059] Drawing 6 shows the condition of having mounted the multichip semi-conductor module 20 shown in drawing 4 in TCP (tape career package). What formed the Au bumps 29 and 29 in the front face of the outermost periphery electrode pads 21 and 21 of a semiconductor chip 15 beforehand as a module 20 is used. These outermost periphery electrode pads 21 and 21 are connected to the Cu leads 26 and 26 attached in the polyimide film 27 by the thimble point bonding method through the Au bumps 29 and 29. And the closure of the laminated-structure, i.e., front face of semiconductor chip 15, side of a module 20 is carried out with resin 28.

[0060] Drawing 7 shows the condition of having mounted the multichip semi-conductor module 20 shown in drawing 4 in the ceramic package. A module 20 is in the condition which turned the semiconductor chip 15 down, and is attached by the connection material 25 in the envelope 30 of a package. The outermost periphery electrode pad 21 of a semiconductor chip 15 and the inner lead (connected with an outer lead 32) which is not illustrated are connected by the wire 22 with the wirebonding method. And this package is sealed by sticking a glass plate 31 on an envelope 30.

[0061] Thus, various products are producible using the multichip semi-conductor module 20 which applied this invention.

[0062] Drawing 8 shows the example which mounted the multichip semi-conductor module 50 with the face down bonding method on PWB (printed circuit board)51.

[0063] This multichip semi-conductor module 50 forms the metal bump 10 who projects at a rear-face side in the semiconductor chip 15 of the lowest layer of the multichip semi-conductor module 20 shown in drawing 4 . That is, a semiconductor chip 15 contacts the rear face of the wiring layer by the side of a front face, and has two or more nickel bumps 10 who project in the rear-face side of a substrate 6 through a through hole. The exposure by the side of each nickel bump's 10 substrate rear face is covered by solder deposit 11B. The semiconductor chips 16A, 16B, 156E, and 16D by which the laminating was carried out on this semiconductor chip 15 are the same as that of what was shown in drawing 4 .

[0064] On the other hand, the electrode pads 17 and 17 which consist of aluminum layer, a Ti/W layer, and an Au layer are formed in the location corresponding to the nickel bump 10 of the above-mentioned semiconductor chip 15 at the front-face side of PWB51.

[0065] Mounting lays PWB51 on a stage, it moves the multichip semi-conductor module 50 horizontally, is positioned in the nickel bumps 10 and 10 of a semiconductor chip 15, --, the location where the electrode pads 17 and 17 by the side of PWB51 counter mutually, and lays it on PWB51. And the nickel bumps 10 and 10 of a semiconductor chip 15 and -- are connected with the electrode pads 17 and 17 by the side of PWB51 through solder 11B by the reflow. Thus, it can mount easily.

[0066] When it becomes clear by the electric test after the completion of mounting that the defect chip is included in the multichip semi-conductor module 50, a defect chip as well as the above-mentioned multichip semi-conductor module 20 can be repaired easily.

[0067] Moreover, this multichip semi-conductor module 50 can raise the packaging density per unit volume, can be excellent in a response characteristic, and can reduce cost, and can lessen constraint on a chip design and a product design.

[0068] In addition, although the deposit of each semiconductor chip metal bump's 10 exposure was set to Au11 or solder 11B in this example, it is not restricted to this and is good also as In, Su, etc. Moreover, although the deposit on the front face of the maximum of the electrode pad 14 was set to Au18, it is not restricted to this and is good also as Zn, nickel, Cu(s), or such combination.

[0069] Moreover, although the rear face of the electrode pad 14 shall be contacted and the metal bump 10 shall be projected in the rear-face side of a substrate through a through hole 7, it is not restricted to this. A metal bump may not be prepared in a through hole 7 side, but you may set up with the height dimension which exceeds the thickness dimension of the above-mentioned substrate to the front-face side of the electrode pad 14. For example, when such a semiconductor chip is accumulated and it constitutes a multichip semi-conductor module, the metal bump who set up to the front-face side of the semiconductor chip of 1 is fitted

into the through hole of another semiconductor chip which consists in this semiconductor chip bottom of 1, and the tip of the metal bump of the semiconductor chip of the above 1 is connected to the rear face of the electrode pad of the semiconductor chip which consists in the above bottom. When it does in this way, like the case where a metal bump is prepared in a through hole side, the packaging density per unit volume can be raised, it can excel in a response characteristic, a defect chip can be repaired, and cost can be reduced, and constraint on a chip design and a product design can be lessened.

[0070]

[Effect of the Invention] As mentioned above, since the semiconductor chip of claim 1 has the metal bump who projects in the rear-face side of a substrate while having an electrode pad in the front-face side of a substrate, it can constitute the multichip semi-conductor module of various classes simply and easily, so that clearly.

[0071] Moreover, since the exposure by the side of the above-mentioned metal bump's above-mentioned substrate rear face is covered by the deposit which consists of an ingredient of the low melting point rather than the above-mentioned metal bump's ingredient, by heating to the temperature which the above-mentioned deposit fuses, the semiconductor chip of claim 2 can connect the above-mentioned metal pad and the electrode pad of another semiconductor chip, and can constitute the multichip semi-conductor module of various classes simply and easily.

[0072] Since it has the multichip semi-conductor module of claim 3 where the semiconductor chip of 1 of claim 1 or claim 2 and another semiconductor chip are able to be accumulated, it can raise the packaging density per unit volume as compared with the case where it once mounts in TCP when arranging a semiconductor chip two-dimensional. Moreover, since a metal bump becomes wiring which connects the electrodes of a chip, the die length of wiring can be shortened as compared with the case where wiring is prepared in the direction of a flat surface, and the response characteristic over a RF can be improved. Moreover, since the connection with the electrode pad of the semiconductor chip which consists in 1 the metal bump and the bottom of a semiconductor chip can be canceled by dissolving the anisotropy electric conduction film used for connection, it can repair a defect chip easily. Moreover, since a laminated structure is formed not in a wafer process but in an assembly process, chip cost can be reduced. And since package bonding of the electrodes of a chip is done by the metal bump, mounting time amount can be shortened. Moreover, without once mounting a semiconductor chip in TCP, each semiconductor chip is accumulated directly and this multichip semi-conductor module is constituted. Therefore, mounting cost can be reduced with chip cost. Moreover, since wirebonding is not performed, an electrode pad may be prepared in the field of the arbitration in a chip, and constraint on a chip design can be lessened. And since the semiconductor chip of various classes can be combined in an assembly process, constraint on a product design can also be lessened few.

[0073] Since it has the multichip semi-conductor module of claim 4 where the semiconductor chip of 1 of claim 2 and another semiconductor chip are able to be accumulated, it can raise the packaging density per unit volume as compared with the case where it once mounts in TCP when arranging a semiconductor chip two-dimensional. Moreover, since a metal bump becomes wiring which connects the electrodes of a chip, the die length of wiring can be shortened as compared with the case where wiring is prepared in the direction of a flat surface, and the response characteristic over a RF can be improved. Moreover, since connection with the electrode pad of the semiconductor chip which consists in above 1 the metal bump and the bottom of a semiconductor chip by heating the semiconductor chip which consists in the above bottom from a rear-face side, and carrying out melting of the deposit which has covered the above-mentioned metal bump can be canceled, a defect chip can be repaired easily. Moreover, since a laminated structure is formed not in a wafer process but in an assembly process, chip cost can be reduced. And since package bonding of the electrodes of a chip is done by the metal bump, mounting time amount can be shortened. Moreover, this multichip semi-conductor module is constituted, combining each semiconductor chip directly, without once mounting a semiconductor chip in TCP. Therefore, mounting cost can be reduced with chip cost. Moreover, since wirebonding is not performed, an electrode pad may be prepared in the field of the arbitration in a chip, and constraint on a chip design can be lessened. And since the semiconductor chip of various classes can be combined in an assembly process, constraint on a product design can also be lessened.

[0074] Since the deposit which consists of an ingredient of the above-mentioned metal bump's deposit and an ingredient which can form an alloy is prepared in the front face of the above-mentioned electrode pad of the semiconductor chip which consists in the above bottom, the multichip semi-conductor module of claim 5 can contact the deposit of the metal bump of the semiconductor chip of the above 1, and the deposit of the electrode pad of the semiconductor chip which consists in the above bottom at the time of assembly, and can be easily connected by performing heating, pressurization, or its both.

[Translation done.]

* NOTICES *

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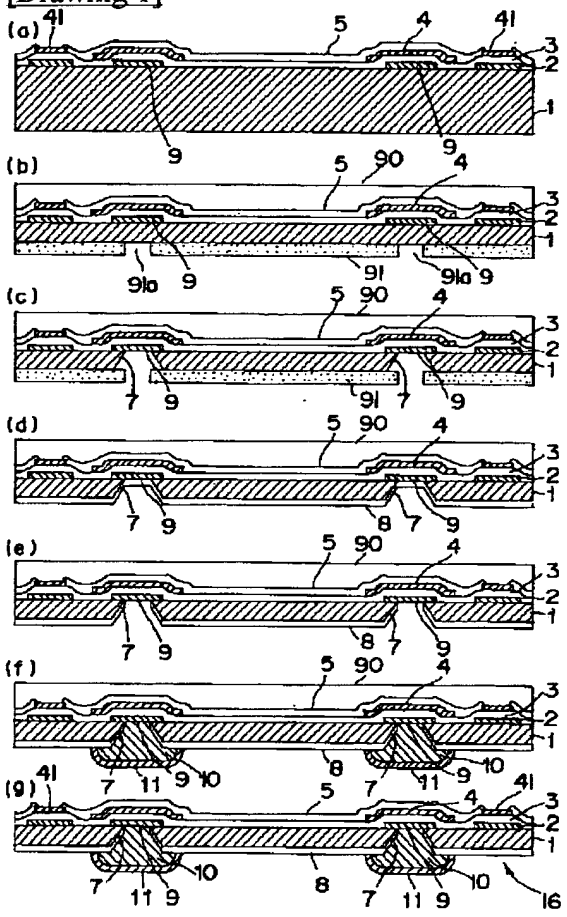
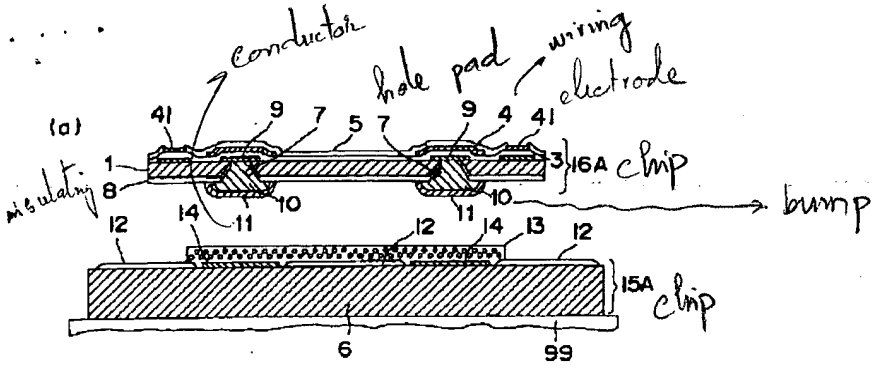
1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DRAWINGS

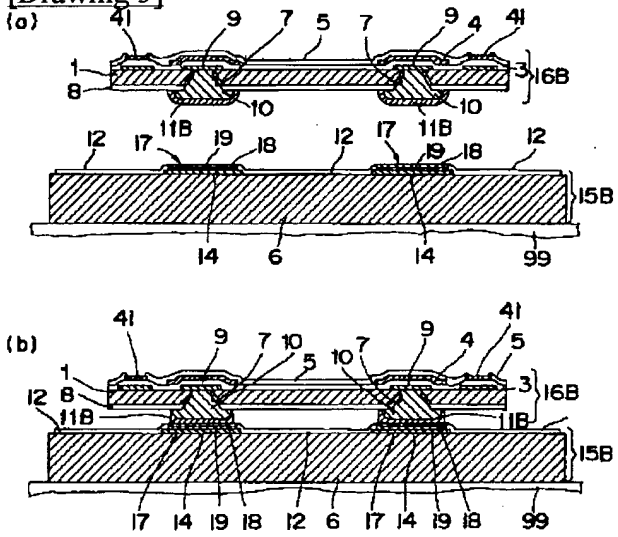
[Drawing 1]



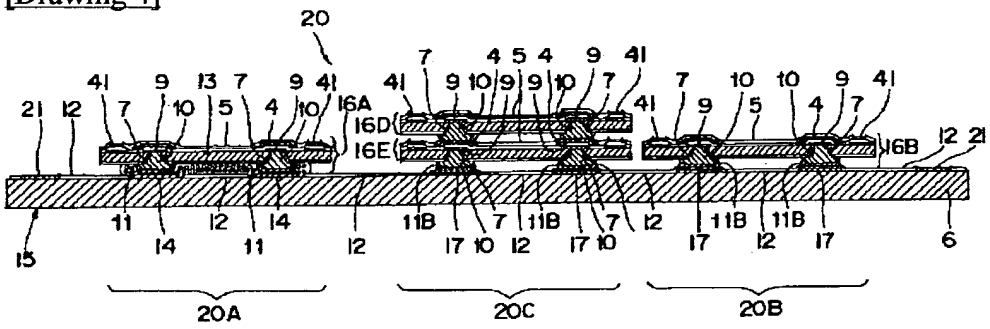
[Drawing 2]



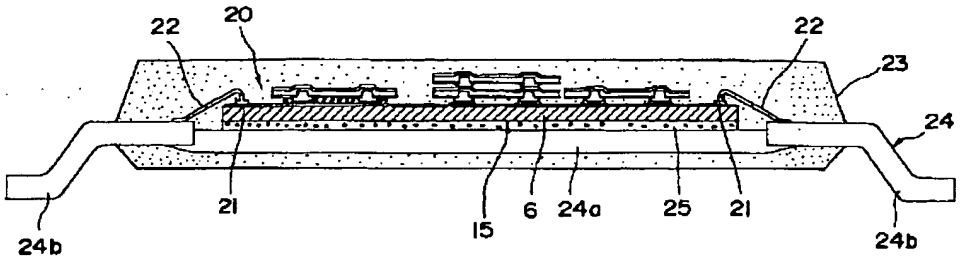
[Drawing 3]



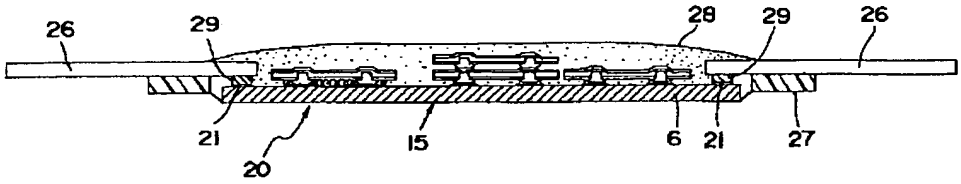
[Drawing 4]



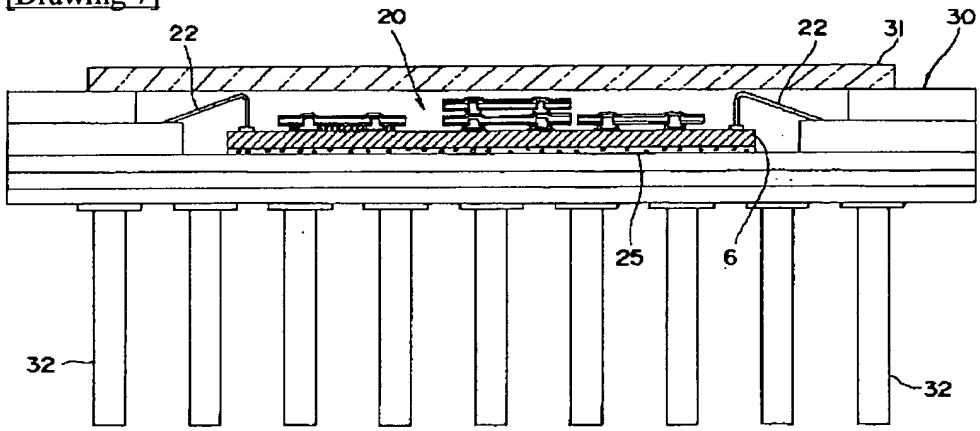
[Drawing 5]



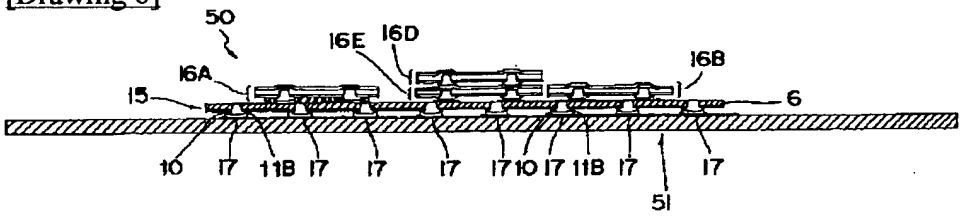
[Drawing 6]



[Drawing 7]



[Drawing 8]



[Translation done.]

* NOTICES *

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is drawing showing the production process of the semiconductor chip of one example of this invention.
[Drawing 2] It is drawing showing the assembly process of the multichip semi-conductor module of one example of this invention.
[Drawing 3] It is drawing showing the assembly process of the multichip semi-conductor module of another example of this invention.
[Drawing 4] It is drawing showing the multichip semi-conductor module of another example of this invention.

[Drawing 5] It is drawing showing the example which carried out the mold of the multichip semi-conductor module of drawing 4 , and mounted it.
[Drawing 6] It is drawing showing the example which mounted the multichip semi-conductor module of drawing 4 in TCP.
[Drawing 7] It is drawing showing the example which mounted the multichip semi-conductor module of drawing 4 in the ceramic package.
[Drawing 8] It is drawing showing the example which mounted the multichip semi-conductor module of another example of this invention in PWB.
[Description of Notations]
1 Six Silicon substrate
7 Through Hole
9, 14, 17 Electrode pad
10 Nickel Bump
11 18 Au deposit
11B Solder deposit
15, 15A, 15B, 16, 16A, 16B, 16D, 16E Semiconductor chip
20, 20A, 20B, 50 Multichip semi-conductor module

[Translation done.]